INTRODUCTION

The recently-released December 2006 edition of the International Technology Roadmap for Semiconductors (ITRS-2006) [1] states that the site flatness of a 300 mm diameter silicon wafer (measured using a Site Flatness Least Squares (SFQR) [2] metric over 26 mm x 8 mm site size) will gradually decrease from 80 nm in 2005 to less than 32 nm in 2013, or even less than 14 nm in 2020. This trend will be combined with increasingly tight edge exclusions (going down to 1.5 mm), improved nanotopography (evolving from 20 nm peak-to-valley, or PV, on 2 mm diameter analysis area to less than 8 nm in 2013 or even 4 nm PV in 2020), and a potential (and controversial) conversion to 450 mm wafer size. These requirements are likely to exceed the capabilities of existing finishing processes, typically consisting of a combination of single and double-sided conventional (i.e., full aperture) polishing processes [3], as well as existing metrology approaches. If technology trends from the optics industry are any indication, sub-aperture polishing processes will therefore be required, along with metrology processes used not only for quality control purposes, but to “feed” these novel polishing approaches.

This paper reports on a collaboration between the National Institute of Standards and Technology (NIST) and QED Technologies®, which combined a wafer thickness metrology using infrared interferometry and polishing using Magnetorheological Finishing (MRF®) to successfully finish 300 mm wafers to unprecedented levels of flatness.

METROLOGY

Optical Wafer Thickness Metrology

In a wafer exposure tool, the wafer is held on a wafer chuck. The wafer flatness at the exposure site is determined by the chuck flatness and the thickness variation of the wafer. Silicon with sufficiently low dopant concentrations is transparent to light at wavelengths larger than 1100 nm. At infrared wavelengths, the thickness variation of silicon wafers, or wafers made from other infrared optical materials, can be characterized using well established optical interferometry methods, that achieve low measurement uncertainties. NIST’s Improved Infrared Interferometer (IR3) is a multi-configuration interferometer, which can be used either with collimated test wave-fronts as a Twyman-Green interferometer, or as a Fizeau interferometer. Figure 1 shows a solid model of the interferometer.

FIGURE 1: NIST Improved Infrared Interferometer (IR3). The main components of the interferometer are: collimator lens (CL), polarizing beam splitter (PBS), phase-shifting reference mirror mount (RM) for the Twyman-Green configuration, diverger lens (DL), zoom lens system (ZL), and camera (CA).

Measurement set-up

IR3 was used in Fizeau configuration for the measurements of wafer thickness variation described in this paper. The wafer was inserted into the test beam of the interferometer as the Fizeau cavity of the interferometer. Reflected light from both wafer surfaces returned to the interferometer’s camera where interferograms were measured. Phase shifting interferometry was accomplished by varying the laser wavelength and the resulting height-maps directly represented the optical thickness variation of the test wafer. The physical thickness variation of the wafer was obtained by
dividing the optical thickness variation by the refractive index of the wafer material. The Fizeau configuration has many advantages for thickness variation measurements. The interferometer cavity is the wafer, a solid, making turbulence absent, and it is unaffected by vibration. In addition, the coherence length of the laser source can be reduced because the distance between the wafer surfaces is small. This completely eliminates coherent reflections from optical surfaces in the interferometer which would otherwise lead to measurement errors.

FIGURE 2: Test end of the IR³ setup for thickness variation measurements of 300 mm wafers. Shown are the collimator lens together with a silicon wafer and a return flat.

MAGNETORHEOLOGICAL FINISHING (MRF®)

MRF is a precision polishing method developed to overcome many of the fundamental limitations of traditional finishing. It is a deterministic finishing process that has the demonstrated ability to produce optical surfaces with an accuracy better than 30 nm peak to valley (PV) and surface micro-roughness less than 1 nm rms on optical glasses, single crystals (such as calcium fluoride and silicon), and glass-ceramics [4,5].

FIGURE 3 Wafer surface is polished in a ribbon of MR fluid.

The shear-mode of removal enables the MRF process to improve micro-roughness, remove sub-surface damage, and reduce residual stress [6,7], which is typically introduced in previous manufacturing steps. The forces acting on the surface are predominantly tangential. The normal forces on the individual abrasive particles are very small (limited to hydrostatic). This is in contrast to conventional polishing techniques where an abrasive is forced into the surface through the action of a lap (either bound or loose). [8] With the conventional lapping process, normal forces can dominate, creating scratches, sub-surface damage, and stress.

MRF is most effective at removing micrometer or sub-micrometer material thickness. There are typically more efficient ways (e.g., grinding, turning, etc.) to remove many tens or hundreds of micrometers of materials. MRF excels at improving surfaces from a few micrometers PV to the limits of what is "measurable" (e.g., 30 nm PV or beyond)—a regime where other commercially available technologies bottom out [9].

MRF integration with existing polishing systems

MRF has the potential to work well with today's wafer manufacturing processes by using it to replace the existing intermediate polishing step in a conventional 3-step finishing process. It can be used to control global total thickness variation on silicon wafers as well as improve the thickness uniformity of the top silicon layer in thick or thin silicon-on-insulator (SOI) wafers[10]. This allows manufacturers to maximize their investments in their conventional equipment while introducing MRF (Figure 4).

FIGURE 4: MRF can be easily integrated into existing manufacturing processes.

RESULTS

Following measurement by NIST, the 300 mm silicon wafers were delivered to QED
Technologies for polishing. All polishing was performed with a standard MRF polishing machine, diamond-based fluid, a 150 mm wheel, and vacuum fixturing (Figure 5).

MRF is based on a magneto-rheological fluid (one whose viscosity varies in the presence of a magnetic field). This process creates an extremely stable and conformable polishing tool. Since the tool is fluid-based, it conforms to any surface shape and eliminates the need for dedicated tooling. One of the benefits of MRF is its insensitivity to moderate (e.g., micrometers of error) part distortion on the mount during polishing [9]. Unlike other technologies where a tool-to-part distance error can result in a one-to-one print-through error, a plunge error into the fluid typically leads to a negligible removal error. Hence, a pin-chucking solution was not required to hold the part. A circular base with vacuum channels cut into the 5 µm flat surface held the part during polishing. As expected, the mounting scheme did cause some distortion of the wafer surface once the vacuum was applied. As seen in Figure 5, the reflection from the wafer surface of a regularly spaced grid highlights the distortion. However, MRF is insensitive to this level of part deformation and no print-through error was measured following polishing.

The wafer was measured in transmission by NIST using the IR3 interferometer, which yields optical path length difference (OPD) information. To obtain the correct wafer thickness variation, as opposed to OPD variation, the data needed to be divided by two times the index of refraction of silicon. The appropriately scaled thickness maps for a sample wafer are displayed in Figure 7, given that $n_{Si} = 3.48$ at the operating wavelength of 1552 nm [11,12]. As shown in Figure 6, the total thickness variation (TTV) was improved from 449 nm to 95 nm. This global TTV improvement of almost 5x was achieved over a 297 mm diameter. The size and rate of the MRF removal function can be optimized to achieve a desired result, such as minimum edge exclusion, minimum cycle time, or minimum flatness.

FIGURE 5a: Vacuum distortion.

FIGURE 5b: Polishing a 300 mm wafer.

FIGURE 6: Wafer thickness variation before and after MRF correction. TTV was reduced from 449 nm to 95 nm over 297 mm aperture (1.5 mm edge exclusion).

FIGURE 7: SFQR Measurement before and after MRF over 25 x 25mm sites. The site flatness improved to better than 20nm over most of the wafer.

Additionally, the site flatness improved to better than 30 nm as shown in Figure 7. As a potential next step, the outliers at the edge and center of the wafer may be eliminated by further process optimization. This is a promising result in light of
the 32 nm site flatness ITRS specification for 2013.

CONCLUSION
This paper has demonstrated that combining advanced metrology, such as the Ir³ interferometer from NIST, with a state-of-the-art sub-aperture polishing process, such as MRF, can successfully address the wafer flatness requirements of many future ITRS technology nodes. It currently appears unlikely that conventional single- or double-sided polishing processes will be able to achieve similar tolerances.

Although the technologies described in this paper represent a technical path forward, a significant challenge remains in creating a cost-effective, commercially viable process. The very low total thickness variation achieved here was demonstrated with several 300 mm wafers, which were MRF polished and measured with the IR³ interferometer at NIST. Cycle times must now be improved to achieve throughput levels consistent with the expectations of the semiconductor industry. This will require not only further development of the polishing process, but specific integration activities with wafer manufacturers to determine where to “stop” the standard (full aperture) polishing process and where to insert MRF (sub-aperture) polishing. Ultimately, the successful integration of these types of novel processes in a very cost-conscious silicon wafer manufacturing industry will indeed depend on the respective economics of this approach versus incumbent technologies.

REFERENCES