DIGITAL PHASE METER FOR MULTIPLE HETERODYNE SIGNALS

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I. Introduction

When fabricating periodic nanostructures using interference lithography, it is essential that the fringes be phase-locked to a small fraction of the fringe period [1]. In our development of scanning-beam interference lithography (SBIL), using a tool known as the Nanoruler [2,3], a digital heterodyne interference fringe control system is utilized to phase-lock the interference fringes to $\pm p/100$ [4]. In this paper we present a digital phase meter that is capable of measuring phases from signals with multiple heterodyne frequencies. The digital phase meter is essential for a novel multiple heterodyne scheme that we are investigating.

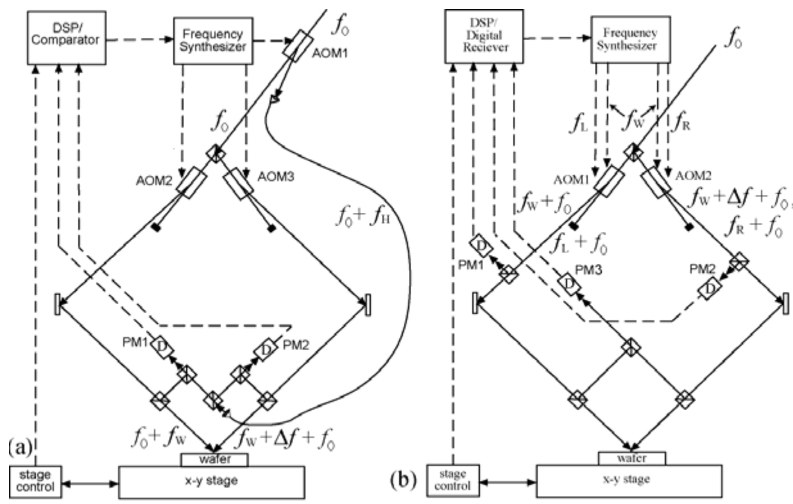

Figure 1. (a) Digital heterodyne interference fringe control system for the Nanoruler. (b) Newly proposed fringe-locking system with multiple heterodyne frequency shifts.

In the present fringe-locking system (Fig. 1a), the two interfering arms are frequency shifted via two acousto-optic modulators (AOM2 and AOM3) to have frequency shifts of $f_W \sim 100$ MHz. A weak reference beam is split off with frequency shift f_H of 120 MHz via AOM1. The two interfering arms are then separately mixed with the reference beam to supply two heterodyne signals of roughly 20 MHz, which are captured by phase meters (PM1 and PM2) and fed to a DSP/comparator. The DSP compares the phase shifts of these two heterodyne signals, together with the interferometer-supplied stage position, to generate an error signal Δf that is fed back into the digital frequency synthesizer to drive AOM3. Changing the cell frequency in AOM3 shifts the light frequency in one arm and thus can lock the fringes to any substrate motion.

In the newly proposed scheme, the frequency synthesizer generates multiple frequencies, so that the left and right arms are shifted with frequencies f_W and f_L, and $f_W+\Delta f$ and f_R, respectively. The amplitudes of f_L and f_R are set to be much smaller than f_W. The two interfering arms then have a heterodyne signal of $f_L - f_R$, measured by PM3, which can be used in the feed-back loop to lock the fringes with error signal Δf. The heterodyne signals $f_W - f_L$ and $f_W - f_R$, measured by PM1 and PM2, respectively, are used to allow correction for dispersion effects in the two arms. In this scheme the image grating will have fringes moving at frequency $f_L - f_R$. By keeping their amplitudes relatively low, they will result as background dose, reducing the contrast of the fringes by an insignificant amount. The detectors are connected to a digital receiver, where the heterodyne signals can be mixed digitally with desired tuning frequencies. The advantage of this scheme is that it eliminates the need for a reference arm, and both the patterning and metrology mode can be combined in one configuration. Future modification of the Nanoruler to multiple beams will also be more feasible.

II. Phase Detection

Phase detection of signals is the main theory behind heterodyne interferometry. The intensity of a signal with three different frequencies recorded by a photo detector is

$$\begin{aligned} I(t) &= \left|E_1(t)+E_2(t)+E_3(t)\right|^2 \\ &= A\Big[1+\frac{2A_1A_2}{A}\cos\left[(\omega_1-\omega_2)t+(\theta_1-\theta_2)\right] \\ &\quad +\frac{2A_1A_3}{A}\cos\left[(\omega_1-\omega_3)t+(\theta_1-\theta_3)\right]+\frac{2A_2A_3}{A}\cos\left[(\omega_2-\omega_3)t+(\theta_2-\theta_3)\right]\Big] \end{aligned} , \qquad (1)$$

where A_i, ω_i, and θ_i are the amplitude, angular frequency, and phase of the i-th signal, respectively, and $A = A_1^2 + A_2^2 + A_3^2$. The intensity consists of three sinusoidal terms oscillating at different heterodyne frequencies, each having a contrast related to the amplitudes of the signals. For conventional heterodyne signals there are only two frequencies, resulting in a single sinusoidal term. The current phase meter is the Zygo ZMI-2001, which detects the phase of a measurement signal by comparing its zero-crossings to those of a reference signal [5]. This operation requires a low-noise signal and is not capable of determining phases from multiple heterodyne signals.

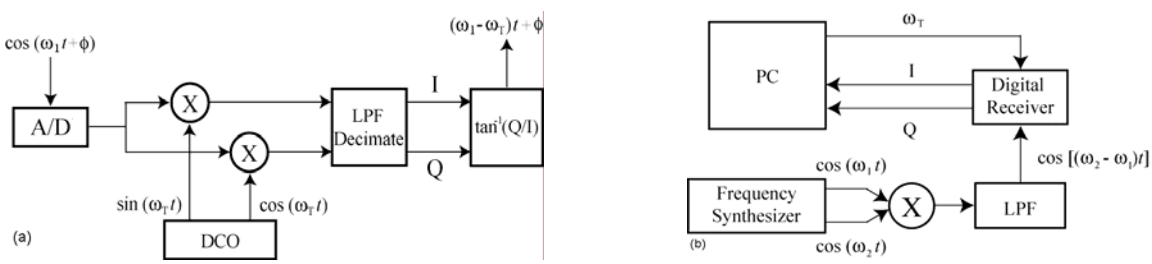

Figure 2. (a) The block diagram for the Pentek 7631 board, performing digital-averaging phase detection. (b) The experimental setup for the digital phase meter.

The digital phase meter we propose operates by a simplified Hilbert-transform phase detection scheme, known as digital-averaging phase detection [6]. We use the Pentek 7631 digital receiver board to perform this function, as shown in Fig. 2 (a). The heterodyne signal is sampled by an A/D and then down-converted to DC by digitally mixing with an in-phase and a quadrature signal at tuning frequency ω_T, generated by the digitally controlled oscillator. The mixed signal is then low-pass filtered (LPF) and decimated, producing signals I and Q. An inverse tangent operation of Q/I will then extract the phase of the input signal. By mixing a single frequency down to DC, the contribution of the other frequencies outside the bandwidth of the LPF can be filtered. Therefore, it will be possible to tune the mixing frequency and extract the phase of a single heterodyne frequency from a multiple heterodyne signal.

Complications arises when the heterodyne frequency being mixed is Doppler shifted due to stage motion, which can be as much as 125 kHz for a stage moving at 50 mm/s with a 400 nmperiod grating. These frequency shifts have to be compensated by changing the tuning frequency of the digital mixer with a phase-locked loop (PLL). The PLL is implemented in software.

III. Experimental Setup

The digital phase meter was tested experimentally, as shown in Fig. 2(b). RF signals generated by a two-channel frequency synthesizer with frequencies of 105 and 95 MHz were mixed in an analog mixer. After filtering with a LPF, the 10 MHz heterodyne signal is input to the digital phase meter setup, which consists of the digital receiver and the PLL controlled by the PC. The software PLL is implemented by difference equations, and its transfer function is shown in Fig. 3. In the figure ϕ_{in}, ϕ_{err}, and ϕ_{out} are the phases of the heterodyne input, the locking signal, and the output signals, respectively, and ω_T is the tuning frequency of the digital mixer. The variables *b* and *c* are control parameters, while $a \sim 1$ is the system gain of the receiver.

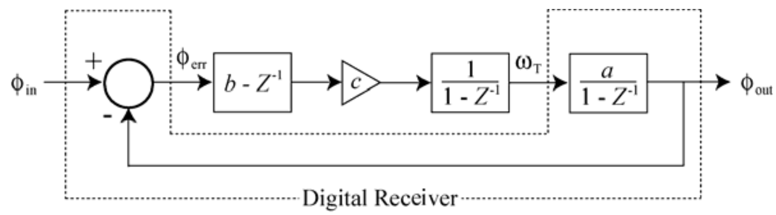

Figure 3. Transfer function of the software phase-locked loop.

IV. Results and Discussion

For a constant frequency shift the input phase signal is a ramp function. The frequency synthesizer has a frequency offset, so that the heterodyne frequency is 10 MHz + Δ*f*. The PLL will be programmed to lock to this frequency offset. The sampling frequency of the A/D is 100 MHz, and then decimated by 4096, for a LPF bandwidth of 24.4 KHz. The bandwidth of the loop is further reduced by a factor of 1024 to ~24 Hz, due to limitations of the memory buffer

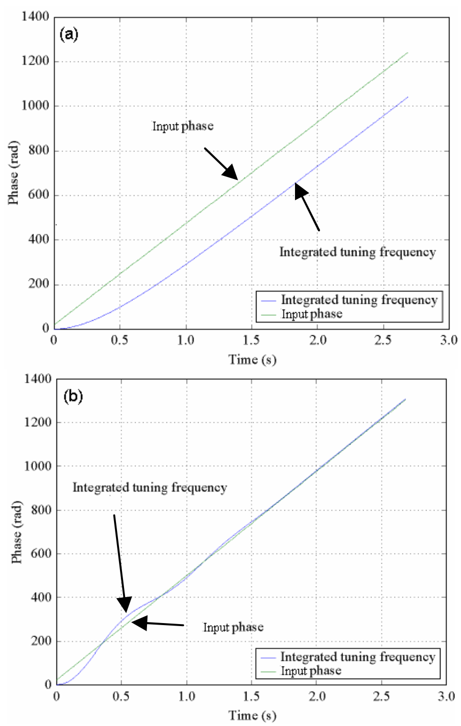

Figure 4. Performance of the PLL locking to (a) frequency, and (b) phase.

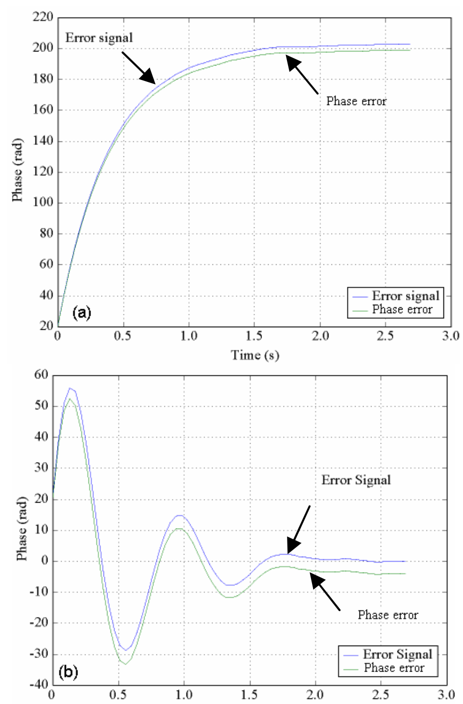

Figure 5. PLL phase error for locking to (a) frequency, and (b) phase.

structure. Two data sets, depicted in Fig. 4 and 5, were taken with c = 7.77, and b = 1 for part (a) and b = 1.05 for part (b). Another set of data is taken simultaneously without the PLL, which represents the input phase. In the first case (Fig 4(a) and 5(a)), the PLL is locking to the frequency, evident as the closed-loop output and input data have the same slope and a constant phase offset. The phase offset can be recovered by adding ϕ_{err} indicated in Fig. 3. In the second case (Fig 4(b) and 5(b)), the PLL is locking to the phase, therefore the close-loop output has no phase offset. The phase data were obtained by integrating the tuning frequency.

The phase errors of the PLL, found by subtracting the close-loop phase from the open-loop phase, are compared to the error signal that the PLL is locking to, as shown in Fig. 5. Ideally the two error curves would agree, and the discrepancies are caused by errors in the system. The system errors are plotted in Fig. 6, and are dominated by numerical integration noise, as the curves closely resemble the tuning frequency. Another significant source of error is the time delay of the PLL. The total accumulated phase error for both cases are ~ 4 radians. The software PLL is running at extremely low bandwidth, and there are random time delays as the digital receiver and the PC are communicating through the PCI bus. The performance of the digital phase meter will be greatly improved by implementing the PLL with hardware such as Field Programmable Gate Array (FPGA) or Digital Signal Processor (DSP).

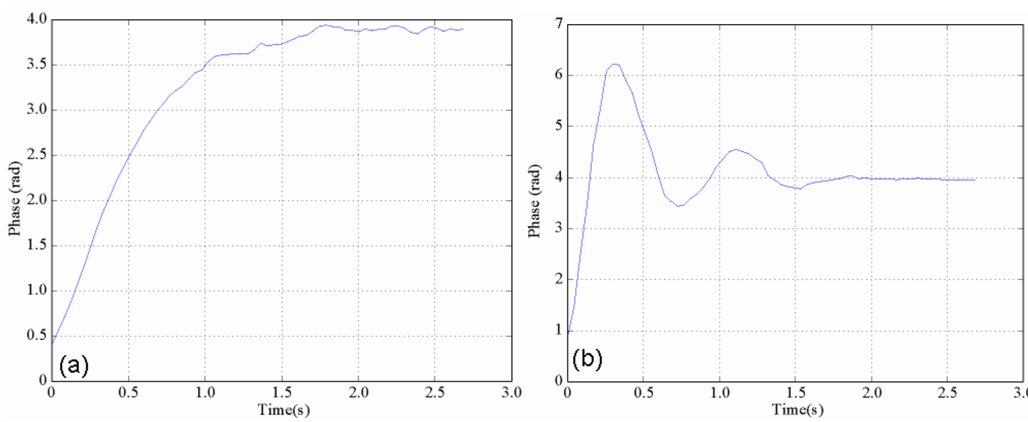

Figure 6. System phase error for locking to (a) frequency, and (b) phase.

V. Conclusion

A digital phase meter capable of extracting phase from multiple heterodyne signals is described. By digital mixing each heterodyne signal can be independently examined while filtering out the others. A software PLL is implemented to adjust for frequency offsets in the signal. The total accumulated system errors are around 4 radians for locking to the frequency and phase. The sources of these errors are mostly due to numerical integration and random time delays in the PLL. The proposed solution to these errors is hardware implementation of the PLL through a FPGA or DSP.

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