

Manufacture of a 150×150 reflective spatial light Modulator integrated directly onto CMOS electronics

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Abstract

This paper presents a micromachined Spatial Light Modulator (uSLM) made by integrating metal MEMS directly on top of planarized foundry-prefabricated complementary metal-oxide semiconductor (CMOS) electronics. Our uSLM consists of both 32×32 (i.e. 1024 segments) and 150×150 (i.e. 22500 segments) array sizes of electrostatically actuated, piston-motion, aluminum surface micromachined mirror pixels. Each mirror segment is addressed through directly integrated CMOS electronics having capable of 4-bit resolution phase control. Technical achievements on manufacturing uSLM such as chemical mechanical planarization, metal-polymer surface micromachining process are discussed.

Introduction

A large-scale SLM has been used for high-speed optical correlation and laser communication applications. Such SLMs can rapidly modulate incident coherent light's wavefront properties such as phase and amplitude. In comparison to classical relatively large and expensive SLMs such as liquid crystal phase devices, MEMS based SLMs have dimension comparable with the wavelength of light, and can be inexpensively fabricated in mass arrays of elements. They also have much faster response times, and higher fill factor, and are not subject to optical problems associated with absorption, diffusion, and polarization effects, which are inherent in liquid crystal devices [1].

Our SLMs function by actuating mirror segments in a surface normal direction over a stroke of up to 1/2 wavelength with a position resolution of one part in 16. To achieve better system performance and packaging advantages, MEMS mirror structure is directly integrated with foundry-prefabricated CMOS driver electronics.

Major technical challenges in this work included: the development of planarization processes for prefabricated CMOS electronics, the development of uniform low stress aluminum sputtering deposition processes and the control of print-through on the mirror segments. The manufacturing process was developed and optimized using a fractional factorial experimentation approach.

System description

Our uSLM consists of seven 32 × 32 and one 150×150 array sizes mirror segments in one prototype chip. Each mirror segment has a stroke of 775nm, which enables to alter the phase of the incident light ($\lambda= 1550\text{nm}$) by up to one wavelength. The device is designed to achieve kilohertz frame rates in a 15mm square aperture. To minimize beam loss, the mirror segment, which is made in aluminum, has optically flat and more than 90% reflective surface. 98 $\mu\text{m} \times 98\mu\text{m}$ size mirror segments are placed on 100 $\mu\text{m} \times 100\mu\text{m}$ pitch, yield a 98% fill factor. Since fabrication uses batch surface-micromachining process, the technology is readily scalable to megapixel arrays with aperture sizes of up to 20cm.

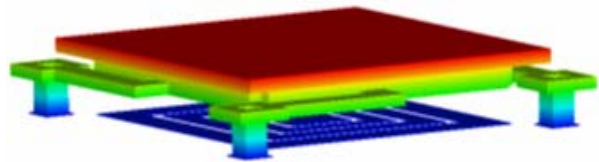


Figure 1. Schematic of a single uSLM segment

Figure 1 illustrates schematic of a single mirror segment. Each mirror pixel is made up of three main components; mirror segment, actuator and electrodes. Mirror sheet is attached into the actuator, which has four folded flexures. The total area of charged electrodes determines the actuator's surface normal positions. The CMOS driver,

which is directly connected to electrodes through small vias, controls the actuator's position by varying the combination of the number of charged electrodes (4-bit, 50nm resolution).

Planarization of CMOS electronics

CMOS driver electronics is custom fabricated by commercial foundry (Austrian Micro Sensors, AMS). Due to existence of multi-layer repetitive deposition and etching processes during CMOS electronics fabrication, the surface of the CMOS electronics shows severely leveled vertical topography. Since further fabrication is performed directly onto the CMOS electronics surface, resulting product will have same surface topography, which is not suitable for our micro mirror applications. To meet the requirements of uSLM, the array should have a RMS figure accuracy and flatness of each segment area of $\lambda/50$ (31nm) and 1nm respectively.

Lee et. al. reported planarization method with additional dielectric layer deposition using RF sputtering followed by subsequent chemical mechanical polishing (CMP) [2]. Further study on planarization process has been done to improve optical quality of the device and better process yields. Additional thick dielectric layer (Si_3N_4) is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD), since CVD coated film shows lower pinhole densities than RF sputtered film. Up to 4um thick Si_3N_4 film is coated using PECVD. Process temperature is less than 100°C, and thickness variation over the individual chip is measured $\pm 10\%$.

Nitride-coated CMOS electronics is subsequently planarized with conventional CMP technique. Pressure Sensitive Adhesive (PSA) tapes are used for mounting die. Double sided adhesive carbon tape (SPI supplies, Product #5083) is inserted between PSA layer and glass plates to minimize tilt-error during die attach process. The glass substrate holding CMOS electronics and force-balancing pieces is polished with 30nm grain size colloidal silica slurries until the desired surface topography is achieved.

Figure 2 (top) shows the surface profile of foundry-delivered CMOS electronics. Interferometric contour mapping microscope (Veeco, WYKO NT2000) is used for the measurement. Measured data show that RMS

flatness is 523.93nm, peak to valley height difference is 2262.92nm. Figure 2 (bottom) shows the surface profile of the planarized CMOS electronics after polishing. As shown in the picture, initial flatness of 523.93nm RMS before planarization (500um scan length) is reduced to 17.65nm RMS. Peak to valley height difference is reduced from 2262.92nm to 112.43nm.

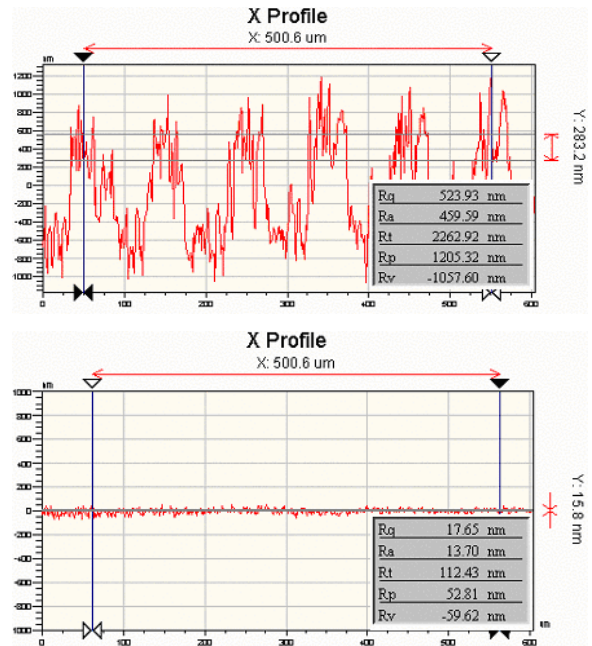


Figure 2. Surface profile of the prefabricated foundry CMOS electronics (top) and planarized CMOS electronics (bottom).

Metal-polymer MEMS fabrication process

Bifano et.al. reported manufacturing process of the 1024 segment large-scale metal MEMS mirror arrays with integrated electronics [3]. Polyimide has been replaced as a sacrificial material rather than photoresist, since photoresist starts to reflow at over 90°C and shows excessive print-through from underlying patterns. Polyimide allows several advantages; such as (1) allows high temperature metal deposition, (2) reduces print-through, (3) allows dry release process rather than wet release which causes possible stiction.

Aluminum is chosen as a structure material, since it allows low cost, uniform film deposition in low temperature and lower voltage activation than the device made of silicon. Also aluminum is a naturally reflective material (more than 90% reflectivity) that meets our

application's requirement. The uniform low stress aluminum sputtering deposition processes are developed by customized deposition chamber and tightly controlled environmental parameters, such as pressure, temperature and RF power.

Integrating MEMS structures on planarized CMOS electronics consists of seven major sub-processes: via cuts/filling, electrode, anchor, actuator, mirror thickener, mirror segment and sacrificial release. Since any topography in structure layers will affect the top mirror layer, maintaining a flat surface in each process step is critical. Also it will prevent the print-through during following fabrication process.

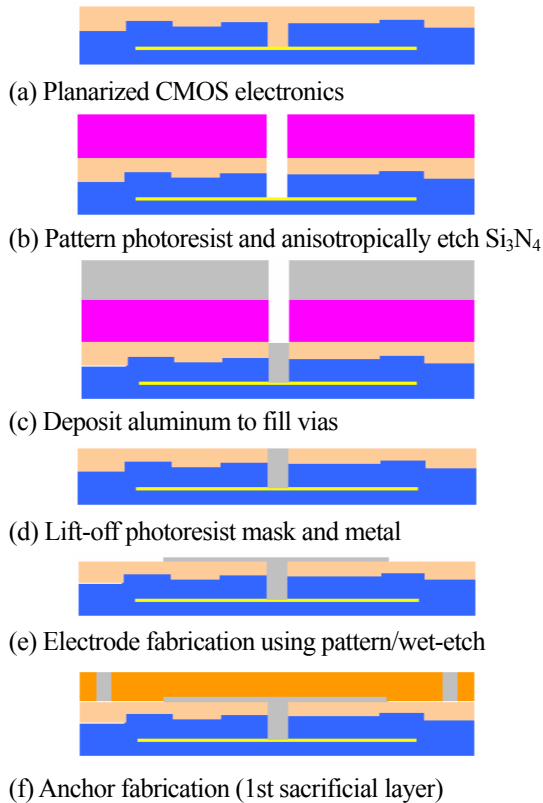


Figure 3. Illustration of via etch/fill, electrode, anchor fabrication process

Vias are anisotropically etched by Reactive Ion Etching and filled through planarized Si_3N_4 layer to create interconnections between electrodes and CMOS driver. Subsequent electrode fabrication is followed by thin metal layer deposition/pattern photoresist mask/wet-etch/cleaning processes.

Actuator anchor is fabricated with similar schemes. To form the surface normal gap between electrode and actuator, the 1st sacrificial layer, polyimide (PI2555) is spun on and cured to yield a normal thickness of $2.5\mu\text{m}$. Metal mask for the anchor is formed by thin metal deposition/pattern photoresist/wet-etch mask metal. The polyimide layer is then anisotropically etched using oxygen plasma. Thick metal deposition is followed to fill the anchor. The bulk of the aluminum and photoresist are then removed by lift-off process (Figure 3).

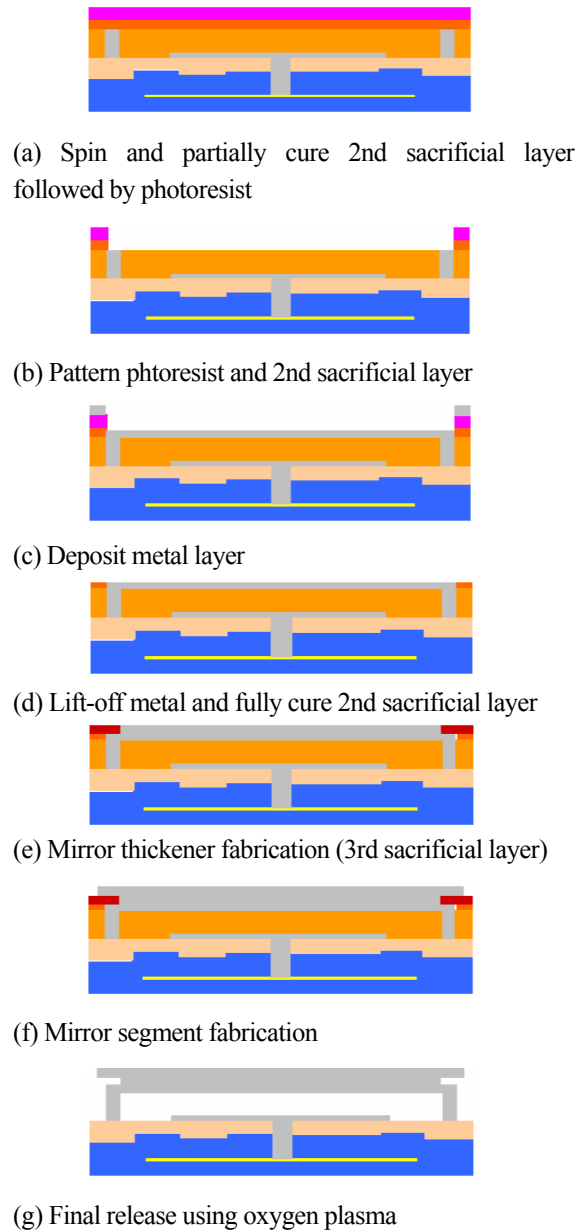


Figure 4. Illustration of actuator, mirror thickener, mirror segment fabrication

The 2nd sacrificial layer, polyimide (PI2556) is spun on to 0.85um thick, then partially cured, allowing the material to be etched by photoresist developer. Photoresist is spun on and patterns the actuator with polyimide using developer. Aluminum is then sputtered to fill the etched actuator pattern. The 2nd sacrificial layer is fully cured after lifting-off the metal and photoresist.

The 0.85um thick actuator thickener as well as the 3rd sacrificial layer (PI2556) is fabricated using the same process used for the actuator. The mirror segment is then fabricated following the 1um thick metal deposition, patterning and wet-etch. After removal of photoresist, the device is fully released by oxygen plasma (Figure 4).

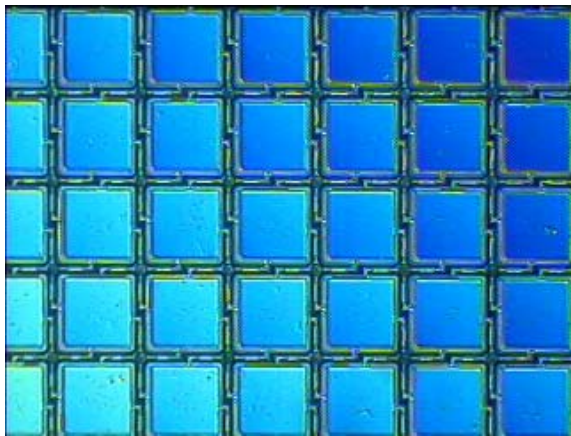


Figure 5. Microscope picture of fully released mirror segments

Figure 5 shows mirror segments after the device is fully released by oxygen plasma. For the evaluation purpose, MEMS structures are fabricated onto the bare silicon substrate, which has the same size as our CMOS electronics die. Figure 5 clearly shows our new process reduces print-through to a great extent. Measurement shows that the print-through in actuator fabrication process is reduced to 50nm from 850nm.

Since the work on via cuts/fill process is still in development at the time of this project, MEMS devices were fabricated on non-planarized CMOS electronics. Electromechanical testing of the fabricated device was performed under a WYKO surface mapping interferometer. As shown in the Figure 6, an individual mirror segment was addressed and deflected with no

cross talk or other influence on its neighboring actuators.

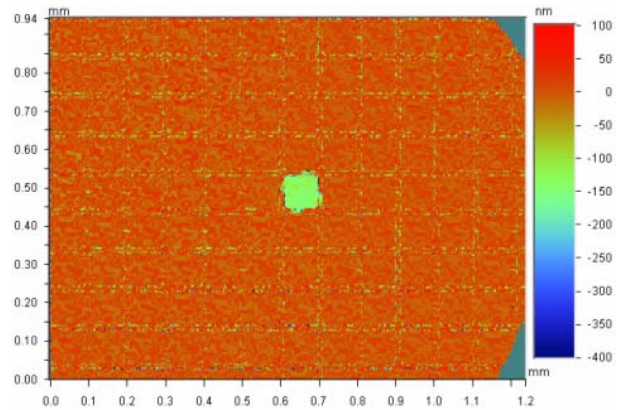


Figure 6. Single pixel addressed with no influence on its neighboring actuators

Conclusion

Technical achievements and challenges associated with manufacturing a large scale uSLM directly integrated on top of the planarized CMOS electronics are described. CMOS electronics is planarized by our chip-scale planarization process using low temperature dielectric material deposition and CMP. A new metal-polymer surface micromachining process to reduce print-through has been developed and we demonstrated an individual pixel actuation by far. The future effort will combine these two successes to produce a large array of uSLM onto the planarized CMOS electronics.

References

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