

SILICON ON INSULATOR (SOI) WAFER POLISHING USING MAGNETORHEOLOGICAL FINISHING (MRF) TECHNOLOGY

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1. INTRODUCTION

The specifications for the top layer of silicon on SOI (silicon-on-insulator) wafers continue to grow tighter. As reported in the December 2001 edition of the International Technology Roadmap for Semiconductor (ITRS-2001), the requirements for absolute thickness and thickness variation of the silicon layer are pushing the limits of both the current metrology and fabrication processes [1]. Traditional manufacturing processes cannot meet the proposed thickness specification (T_{si}) of 20-50 nm and associated thickness variation of $\pm 5\%$ of the T_{si} . The ITRS-2001 predicts that these requirements will become increasingly difficult to meet as absolute thickness specification (T_{si}) drops to 20 nm with an allowable thickness variation as low as 2 nm peak-to-valley. Magnetorheological finishing (MRF) is uniquely able to target the absolute thickness of the silicon layer while significantly, and simultaneously, improving its thickness variation. This paper will describe MRF and its viability as a manufacturing solution, allowing wafer fabricators to reach the current, and future, SOI specifications. Initial results obtained using the MRF process on SOI wafers will be demonstrated.

2. MRF PROCESS

Magnetorheological finishing (MRF) is a deterministic, final figuring process developed to address many of the limitations encountered in traditional polishing. The three key components to deterministic polishing processes are 1) a stable polishing tool, 2) repeatable and reproducible metrology data, and 3) software to de-convolve the metrology error map and the removal rate of the polishing tool to obtain an accurate dwell schedule. The MRF polishing tool is based on a magnetorheological fluid whose viscosity is changed significantly in the presence of a magnetic field. Using MR fluid as a polishing tool presents significant advantages compared to other sub-aperture polishing approaches, including the ability to adjust removal rate and the insensitivity to z-axis positioning [2]. There are several parameters which can be controlled to increase or decrease the removal rate of the polishing tool (e.g., magnetic field, depth into fluid, viscosity of fluid, and wheel speed.) Figure 1 displays an SOI wafer while being polished with the MRF.

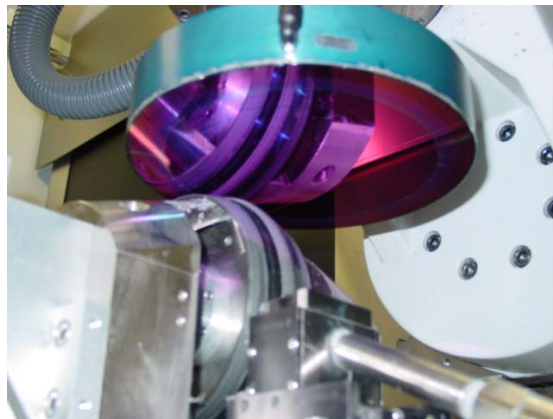


Figure 1. Image of an SOI wafer being polished with the MRF process. The wafer is held with vacuum on a New Way Precision chuck [3].

The MRF process has been successfully implemented in the fabrication process of high quality lithography optics and many other applications [4]. While achieving less than 0.5 nm rms micro-roughness, surface figure error below 2 nm rms is simultaneously reached on various types of optical glass (such as BK7 and SiO₂) and single crystal materials (such as silicon and CaF₂) [5]. Typically for these types of optical components, the primary advantages of MRF are associated with its very deterministic nature and ability to polish a wide range of geometries (flat, spheres, aspheres, cylinders, etc.) to an unprecedented level of precision in a fast and cost-effective manner. For most optical applications, MRF is typically used to shape a lens based on reflected or transmitted wavefront metrology. In the case of SOI wafers, on the other hand, it is the thin film of Si on top of a SiO₂ layer (itself on a silicon layer) for which thickness and thickness uniformity needs to be improved.

3. SOI THICKNESS MEASUREMENTS

Standard methods to measure the thickness and thickness variation of the top silicon layer of SOI wafers are reflectometry and ellipsometry [6]. For work done in this research, thickness and thickness variation measurements were made using spectral reflectometry with an ADE AcuMap II tool [7]. Using this equipment, measurements were made over the entire surface and sampled every millimeter, producing over 20,000 data points for a 200 mm diameter wafer in under a few minutes. Repeatability of these measurements was estimated to be approximately 0.5 Å variability. While techniques such as ellipsometry may be even more accurate, the measurement cycle time is much higher and the number of measurements on the surface are much fewer (typically 125 points per surface). At this low data density, some surface errors can be easily missed.

4. MRF on SOI PROCESS

The final goal of this research was to produce an SOI wafer with a silicon thickness of 20-50 nm and associated thickness variation less than 5% of the nominal thickness. The goal consists of two separate tasks: nominal thickness reduction and thickness variation correction. The deterministic nature of the MRF process can very effectively address both tasks. A precise CNC machine was used to position the SOI wafer into the MR fluid ribbon. The wafer is held onto a porous ceramic chuck using vacuum (see Figure 1). In most cases, SOI wafers have an initial silicon thickness ranging from $T_{si} = 50-100$ nm and a uniformity of 5% of the T_{si} . With initial conditions such as these, one approach to meet the desired SOI specification is to divide the MRF polishing into two iterations. The first iteration is designed to bring the thickness close to the desired thickness, but with enough material remaining to perform a second iteration. The first iteration can be conducted with minimal metrology performed on the wafer. If the process used to fabricate the wafer produces repeatable thickness values, then initial metrology would not be necessary. The second iteration is designed to reduce the thickness to the final desired thickness and simultaneously correct the thickness variation. This second iteration, on the other hand, requires that metrology be performed prior to MRF. For the initial process investigation and development, the two tasks were conducted separately.

5. INITIAL RESULTS

The first step was to determine how accurately the MRF process could achieve a given thickness. As mentioned earlier, the first polishing iteration was performed to reduce the silicon thickness to just above the desired thickness while leaving enough material for the second iteration. Figure 2 displays an example of radial average thickness results before and after MRF polishing of a 200 mm diameter wafer.

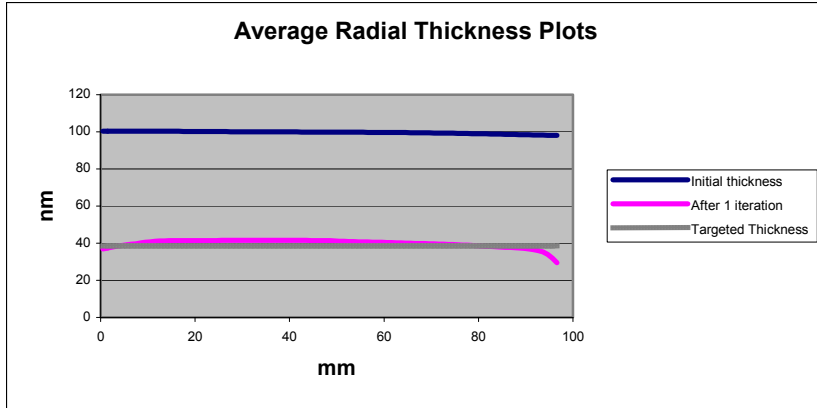
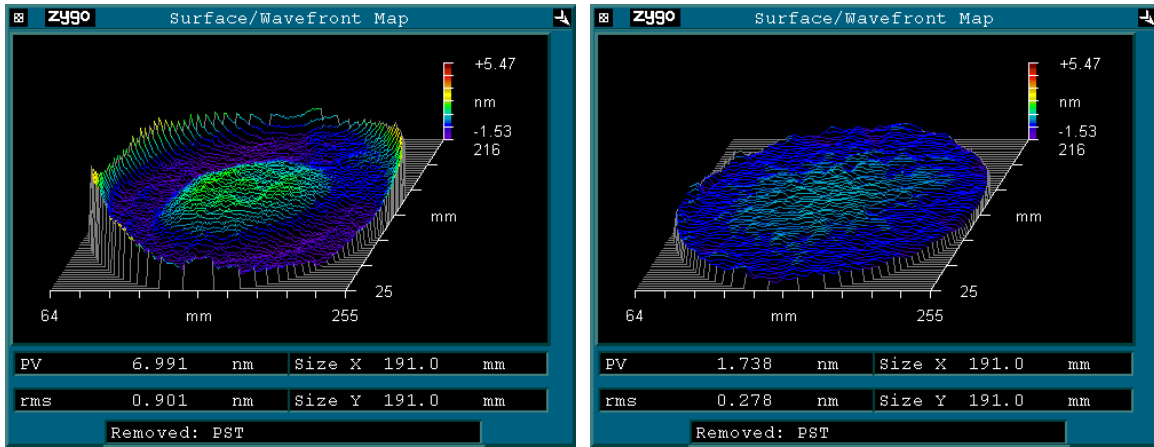


Figure 2. Silicon thickness measurements (with 2.5 mm edge exclusion) made before and after a MRF thickness reduction run.

The initial average thickness of the silicon layer was 99 nm as measured with the AcuMap II. The goal was to remove three-fourths of the material required to reach the 20 nm thickness target. With no metrology input, the MRF was programmed to uniformly remove a total of 55 nm from the “thinnest” area of the silicon layer. This set the target thickness to 38 nm. The resulting average silicon thickness following 37 minutes of MRF polishing was 39 nm. For this iteration, the error in thickness reduction was less than 2%. This result demonstrates the ability of the MRF process to very precisely target and reach a defined thickness.

The second task was to reduce the thickness variation of the silicon layer. The approach used to correct the thickness uniformity of the silicon layer was to change the process parameters to reduce the typical removal rate of the MRF process to a lesser removal rate. Figure 3 displays the thickness variation results of the silicon layer before and after MRF processing.



(a)

(b)

Figure 3. Silicon thickness variation measurements made (a) before and (b) after MRF processing with reduced removal rate.

The results show that the thickness variation was reduced from 7 nm to below 2 nm peak-to-valley, and even more impressively, achieving less than 0.3 nm rms even with the high-density measurement made with the AcuMap II. The total cycle time of the polishing run was 46 minutes. Work is currently being performed to achieve similar or improved uniformity results using more aggressive removal

settings. Initial results show that the uniformity correction cycle time can be reduced to less than 5 minutes.

6. CONCLUSION AND RELEVANT WORK

From the initial series of experiments performed using the MRF process on SOI wafers, the results show that the MRF process can successfully achieve the desired silicon thickness of 20-50 nm while reducing the thickness variation to less than 5% of the T_{Si} . Currently, work is being performed to combine the two separate tasks (reducing silicon thickness and correcting thickness variation) on a single operation.

In parallel, work is being performed on “thick” SOI and prime silicon wafers. Thick SOI wafers typically have a silicon layer thickness of several microns and again a uniformity of 5% of the T_{Si} . The approach to implement the MRF process for this type of wafer is different from the “thin” SOI process presented here. For this application, the parameters are adjusted to produce a more aggressive removal rate, as the amount of desired material removal is on the order of microns, versus ~50-70 nm removed for thin SOI wafers [8].

Investigations have also been performed to quantify many other additional important aspects of polishing Si or SOI wafers, including roughness, cycle time, contamination, process integration issues, etc. Initial findings have verified that MRF meets or exceeds industry standards in these areas and is a viable manufacturing solution for SOI wafer fabrication [8].

7. REFERENCES

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