

Atomic Force Microscopy of Semiconductor Line Edge Roughness

Ndubuisi G. Orji, Theodore V. Vorburger[†], Jay Raja

The University of North Carolina at Charlotte, Charlotte, NC 28223

[†]National Institute of Standards and Technology, Gaithersburg, MD 20899

1. Introduction

Over the last two decades the width of patterned lines on semiconductor devices has continuously decreased. Based on technology trends predicted by the International Technology Roadmap for Semiconductors (ITRS) [1], the linewidth of isolated gate lines on microprocessors will be reduced to less than 50 nm by 2012. This trend towards smaller feature sizes poses a great challenge to the tools, analysis methods, and calibration techniques used in linewidth measurements. State-of-the-art linewidth measurement involves the use of scanning electron microscopes (SEM), but as the feature sizes decrease, SEM techniques may become inadequate for such measurements.

Part of the difficulty of imaging patterned lines with the SEM lies with the uncertainties associated with determining the edges of lines; this can be attributed partly to the deviation of the line edge from the mean line, otherwise known as line edge roughness (LER). Another important part of the problem lies in the fact that the decrease in LER is not proportional to feature size as the industry move toward smaller features because the fundamental causes of LER are material and process dependent rather than size dependent [2]. Errors in the range of ~25 nm which were acceptable for linewidths of 500 nm or more will consume over half the lithography error budget for 100 nm linewidths and below [3].

Recent studies have correlated LER with increased current leakage [4,5] for linewidths below 100 nm, and thus highlight the need for an in-depth characterization of this parameter. This work explores the use of atomic force microscopes (AFM) for characterizing LER. The challenges involved with AFM characterization of LER are highlighted, and various scanning strategies and analysis techniques are presented. The objective of this work is to present some of the measurement and analysis techniques needed to extract valuable LER information using the atomic force microscope.

2. Imaging Technique

The atomic force microscope since its introduction [6] has gained wide usage in surface topography measurements at the very small scale. The ability of the AFM to produce three-dimensional maps at the nanometer scale has greatly increased its popularity as an imaging tool. The application of precision engineering principles in the construction and characterization of the AFM have also increased its usefulness as a metrology tool [7,8]. In addition to a variety of uses, it is increasingly being used as a process control tool, especially in the semiconductor industry, where it has become a major enabling tool in the measurement of very small features. In spite of the high resolution of the AFM and its increasing use in research and industry, the scanning electron microscope is still the imaging tool of choice in the semiconductor manufacturing industry. The depth-of-focus, high precision ($< 0.7\text{nm } 3\sigma$), and throughput of the SEM, make it especially attractive as a process control tool. However, as feature sizes get smaller, the SEM may no longer have the required resolution needed to measure certain parameters. One such parameter is LER, which the ITRS has set a long term target of reducing to 0.9 nm by the year 2013 [1]. The ITRS

defines LER in terms of linewidth variation over a range of four technology nodes, using all frequency components. This target is ambitious, and the ITRS indicates that at present there is no known method of achieving or verifying this target. One of the few tools with the resolution needed to characterize the LER down to the levels indicated on the roadmap (a short term target of 2.7 nm by 2006) is the atomic force microscope. Under optimum conditions the AFM can measure surfaces and features with sub-nanometer resolution. The use of the AFM as a process control tool of choice is perhaps a few years away, but this tool can be used in conjunction with other techniques and tools to perform an in-depth study of LER with the aim of understanding the origins, characterization methods, important spatial wavelengths, and correlation with performance. As much promise as the AFM holds for characterizing LER, there are some challenges. These include the inaccessibility of the tip to the sidewall, tip dilation (tip broadening), and errors due to non-conventional scanning strategies. A word on terminology, there is an ongoing debate on what term best describes line edge roughness. In some cases it is used interchangeably with linewidth uniformity, and sidewall roughness. We assume LER to be a general term. We use the term linewidth uniformity to represent deviations in linewidth as shown later in figure 3, and sidewall roughness to represent similar deviations, but for a single side. The techniques described are for measuring both parameters.

Here we present a combination of AFM measurement methods, and analysis techniques we are researching to acquire accurate images of the line edge and sidewall of semiconductor features. Conventional AFM imaging involves scanning the tip across the surface as shown in figure 1. The problem with this configuration when it comes to measuring sidewall roughness is that little or no sidewall information is obtained, in addition, tip dilation makes it almost impossible to image the line edge without errors. Slightly tilting the sample allows easier access to the sidewall. Most conventional AFM tips have an asymmetric cone angle (for example with front and back angles of 25° and 10° respectively, and 17° on each side), so depending on the sample tilt angle the image can be limited by the sidewall of the tip. A judicious selection of the scanning direction is required when using such a tip. To alleviate this problem we are using very sharp tips that have a more uniform conical shape. To gain increased access to the sidewall, one can also tilt the cantilever. Tilting the cantilever may not be as easy as tilting the sample, since this may require tilting the whole cantilever holder. Figure 1 shows some possible configurations.

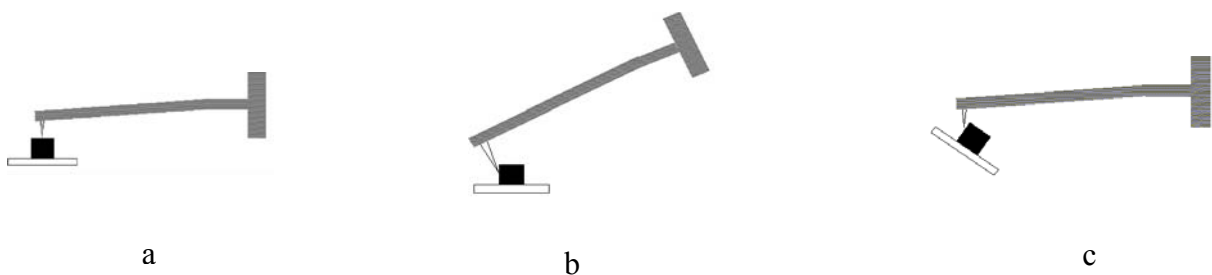


Figure 1 show possible AFM probe configurations (a) in conventional AFM imaging configuration, (b) cantilever slightly tilted and (c) with the sample holder tilted.

The methods outlined above will allow imaging of both the sidewall and the line edge, though only one side of the feature is being imaged.

If one is interested in only the sidewall, and one's system allows it, rotating the sample 90° is an option. This configuration is destructive because the sample must be cleaved to allow the tip unrestricted access to the sidewall. Figure 2 shows a schematic of such a configuration. In addition to sharp tips, we intend to take images using special cantilevers where the tips are at an angle.

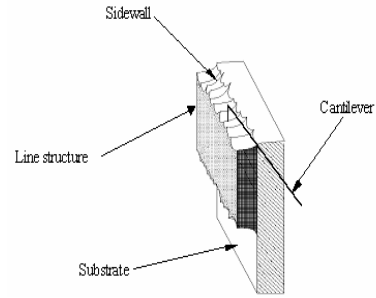


Figure 2 A schematic of a line structure rotated 90° for easy access to the sidewall.

3. Analysis Technique

In analyzing LER, analysis methods emphasizing different spatial frequency ranges maybe needed for the different types of linewidth uniformity and sidewall roughness. Also of great interest is the question of whether linewidth uniformity and sidewall roughness are correlated, and if so how. Since the SEM is the imaging tool of choice in the semiconductor industry, some of the most useful analysis techniques for AFM LER data will be those that can easily be correlated with the data taken with the SEM. Perhaps the most used technique is the rms roughness shown in equation 1 where δ is the deviation from the average line edge. In this case it is calculated as three standard deviations (3σ) of the values.

$$LER = 3\sigma = 3\sqrt{\frac{N\sum\delta^2 - (\sum\delta)^2}{N(n-1)}} \quad (1)$$

This can easily be applied to the data acquired using the techniques outlined above. Another technique [9] is to calculate the non-uniformity of the whole line structure. This method uses both sides of the line structure, so it cannot be used on data acquired by some of the techniques outlined above, but where possible gives a good indication of the uniformity of the line structure, and yields results that can easily be compared to information obtained from the SEM.

In order to obtain the type of data sketched in Figure 3, one has to determine where the line edge is, since the line profiles are likely to have rounded corners due to tip dilation. We will apply a geometric filter [10,11] to remove the influence of the tip. In this case the linewidth uniformity of the line will be calculated at a specified vertical threshold, a method employed in [12], we will also evaluate the influence of various threshold levels



Figure 3 A top down image of a line structure. Showing Linewidth uniformity

on the results. The results obtained will only give linewidth uniformity and not sidewall roughness, but will give a very good indication of uniformity and quality of the line structure. This is also the definition used by the ITRS [1], which proposes the use of all frequency components and both edges, and evaluated over four semiconductor technology nodes.

4. Planned experimental work

We are currently taking measurements using a commercial AFM. We are measuring patterned lines of approximately 250 nm linewidth so we can first verify the utility of some of our techniques before using smaller, more expensive samples. A high-aspect-ratio conically shaped tip is being used. We intend to examine the influence of various tilt angles on the data, and what tilt angles give the “best” results. We also intend to obtain specially made samples with roughness of known values, and spatial frequencies.

Acknowledgements

This work is supported in part by the Office of Microelectronics Programs (OMP) at NIST. The authors are grateful to A. Vldar and J. Martinez for their careful reading of the manuscript.

References

1. The International Technology Roadmap for Semiconductors (ITRS) 2001, Semiconductor Industry Association, San Jose (2001)
2. G. P. Patsis, A. Tserepi, I. Raptis, N. Glezos, and E. Gogolides and E. S. Valamontes. Surface and line-edge roughness in solution and plasma developed negative tone resists: Experiment and simulation, *J. Vac. Sci. Technol. B* 18 (6), Nov/Dec 2000
3. A. E. Braun, CD-SEM: Precision or Accuracy, *Semiconductor International*, Feb 1999.
4. C.H. Díaz, H-J Tao, Y-C Ku, A. Yen, and K. Young, An Experimentally Validated Analytical Model For Gate Line-Edge Roughness (LER) Effects on Technology Scaling, *IEEE Electron Device Letters*, Vol. 22, No. 6, June 2001
5. K. Patterson, J. L. Sturtevant et al, Experimental determination of the impact of polysilicon LER on sub-100-nm transistor performance. *Proc. SPIE Vol. 4344*, 809-814 (2001).
6. G. B. Binnig, C. F. Quate, and Ch. Gerber, Atomic force microscope. *Phys. Rev. Lett.*, (12)
7. J. E Griffith, D. A. Grigg, Dimensional metrology with scanning probe microscopes *J. Appl Phys.* 74 (9) R83 (1993)
7. R. Dixon, R. Koning, V. W. Tsai, J. Fu, T. V. Vorburger ; Dimensional metrology with the NIST calibrated atomic force microscope. *Proc. SPIE Vol 3677*, 21-2 (1999)
8. Winkelmeier S, Sarstedt M, Ereken M, et al., Metrology method for the correlation of line edge roughness for different resists before and after etch., *Microelectron Eng* 57-8: 665-672 (2001)
9. V. Srinivasan, Discrete morphological filters for metrology. *Proc. 6th IMEKO ISMQC symposium on metrology for quality control and production*, TU Wien, Austria, 1998
10. Villarrubia, J.S., Algorithms for scanned probe microscope image simulation, surface reconstruction, and tip estimation. *J. Res. NIST*, 102(4), 425-454, (1997)
11. C. Palmateer SC, Forte AR, et al, Comparison of metrology methods for quantifying the line edge roughness of patterned features, *J Vac Sci Technol B* 17: (6) 2488-2498 (1999)