First Call for Papers

ASPE 2008 Spring Topical Meeting

Precision Mechanical Design and Mechatronics for Sub-50nm Semiconductor Equipment

April 7 & 8, 2008
Berkeley, California

Meeting Co-Chairmen:

John S. Taylor
Lawrence Livermore National Laboratory
Jan van Eijk
Delft University of Technology

Technical Committee:

Chris J. Evans, Zygo Corporation
Pete Fitsos, Lawrence Livermore National Lab.
Stephen J. Ludwick, Aerotech, Inc.
Robert-Han Munnig Schmidt, TU Delft and ASML
Senajith B. Rekawa, Lawrence Berkeley National Lab.
Marcel J. M. Renkens, Philips Applied Technologies
Jeffrey W. Roblee, AMETEK - Precitech, Inc.
David L. Trumper, MIT
Marek Zywno, KLA-Tencor

The 2008 Spring Topical Meeting will follow the format of its successful predecessors, and will span two days of technical presentations and poster papers, with time allocated for professional networking. **Presenters must submit a 4-6 page extended abstract in advance of the meeting for inclusion in the Proceedings.**

The deadline for submission of short abstracts is February 15, 2008. For additional details and deadlines please check our web site.

For additional information please contact:

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The system error budgets for controlling critical dimensions (CD) and overlay during semiconductor processing lead to astonishingly small numbers for individual elemental errors including stages, alignment, long- and short-term stability, servo-control, and thermal management. The 3-sigma sum of numerous error terms for placing a pattern onto a wafer is typically a small fraction of the nominal critical dimension. As the lithography and related industries move to CD's less than 50 nm, it is important to assess the precision engineering community's ability to meet these increasingly stringent requirements.

The objective of this meeting is to enable a technical dialogue between engineers directly supporting the semiconductor industry and the broader field of precision engineering. The focus of this meeting will be on issues regarding precision mechanics and control, recognizing that detailed issues of lithographic processing, such as resist development, are well-represented in other venues. The intended semiconductor technology audience includes current lithography tool makers, and also related processing requirements, such as mask writing, opto-mechanics, and future technologies such as EUV, maskless, and nano-imprint lithographies.

Contributed papers are invited, but not limited to, the following relevant topics:

- CD and overlay error budgets
- Motion control and synchronization in step-and-scan lithography
- Actuator and sensor innovation
- Motion control requirements for nano-imprint and other new processes
- Stage design and control for high-g and high throughput requirements
- Thermal management
- Precision engineering in a vacuum environment
- Reticle and wafer chucking
- Sensors for alignment and active motion control
- Challenges for cleanliness
- Advanced control strategies
- System qualification and reliability
- Qualification of ultra-precision stages and the application of Standards
- Fixturing of optical components
- Measurement and control of vibration and settling time
- Active and passive strategies for damping
- Metrology and diagnostics of errors
- Alignment of the mask stage, wafer stage, and imaging optics

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